REMARKS

An Excess Claim Fee Payment Letter is submitted herewith to cover the cost of any excess claims added by this Amendment.

Claims 29-39 and 41-57 are all the claims presently pending in the application. Claims 29-30, 41, 45-46 and 49 have been amended to more clearly define the invention. Claims 55-57 have been added to claim additional features of the invention. Claims are 29, 41 and 45-46 independent.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 29-36, 41-42 and 45-54 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ohata, et al. (U.S. Patent No. 4,837,186). Claims 37-39 and 43-44 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ohata, et al., in view of Tanaka (Japanese Patent No. 10-303385).

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

The claimed invention (e. g., as recited in claim 29) is directed to a semiconductor device including a bulk silicon region comprising single crystal silicon, and a silicon-on-insulator (SOI) region. Further, the SOI region includes an insulator layer which is formed beneath an upper portion of the single crystal silicon and has at least one lateral end portion adjacent to a lower portion of the single crystal silicon; and at least one isolation oxide formed in the upper portion of the single crystal silicon so as to form at least one island of the single crystal silicon on an upper surface of the insulator layer.

Importantly, the upper portion of the single crystal silicon comprises crystallized epitaxial silicon which is grown from the lower portion of the single crystal silicon such that the upper portion and the lower portion comprise a same silicon crystal. Importantly, the upper portion of the single crystal silicon is substantially devoid of a defective region.

Conventional substrates having an SOI region are often formed by separation by

implantation of oxygen (SIMOX). However, it is well known that the high energy implantation of the SIMOX process results in a very high defect count per unit area (i.e., defect density) in the silicon over the insulation layer (Application at page 5, lines 2-6). Thus, such conventional devices do not include an upper portion of single crystal silicon which is substantially devoid of a defective region.

Other conventional substrates having an SOI region are formed by a cladding (e.g., wafer bonding) process where an oxide layer is formed in a first surface of a first substrate, a second substrate is bonded to the first surface, and elements are then formed in the second substrate. However, two wafers are bonded together, and so such conventional substrates necessarily are formed of two silicon crystals. That is, such substrates do not have an upper portion and lower portion of single silicon crystal which are formed of the same silicon crystal.

The claimed semiconductor device, on the other hand, includes an upper portion and lower portion of single silicon crystal which are formed of the same silicon crystal (Application at page 9, lines 4-22), and further, the upper portion of single crystal silicon is substantially devoid of a defective region (Application at page 5, lines 8-10). Therefore, the claimed invention provides superior characteristics over substrates which are formed by either the SIMOX (e.g., see Application at page 5, lines 2-10) or cladding process.

II. THE PRIOR ART REFERENCES

A. The Ohata Reference

The Examiner alleges that Ohata makes obvious the claimed invention of claims 29-36, 41-42 and 45-54. Applicant submits, however, that there are elements of the claimed invention which are neither taught nor suggested by Ohata.

Ohata discloses a substrate having an SOI region which is formed by a well known cladding (e.g., wafer bonding) process. The silicon semiconductor substrate includes a first silicon plate, an insulating layer embedded in the first silicon plate so that the surfaces of the silicon plate and the insulating layer are in a mirror surface, and a second silicon plate united with the first silicon plate and the insulating layer at the mirror surface of the first silicon plate and the insulating layer (Ohata at Abstract).

However, Ohata does not teach or suggest "*wherein said upper portion of said single*

crystal silicon comprises crystallized epitaxial silicon which is grown from said lower portion of said single crystal silicon such that said upper portion and said lower portion comprise a same silicon crystal", as recited, for example, in claims 29, 41 and 45- 46.

As explained in the present Application, unlike conventional substrates which are formed by either a SIMOX or cladding (e.g., wafer bonding) process, the claimed invention, may form an upper portion of single crystal silicon is formed over an insulator layer by depositing amorphous silicon on the insulator layer and the lower portion of the single crystal silicon, and crystallizing the amorphous silicon by using said lower portion of the single crystal silicon as a crystal growth seed (Application at page 7, line 6-page 8, line 11). Thus, the claimed invention includes an upper portion and lower portion of single silicon crystal which are formed of the same silicon crystal (Application at page 9, lines 4-22). Therefore, the claimed invention provides superior characteristics over substrates which are formed by either the SIMOX (e.g., see Application at page 5, lines 2-10) or cladding process.

Further, it is well-known that a substrate prepared by a cladding process involves two silicon crystals bonded together. The cladding process requires many steps and therefore, the resulting substrate is expensive. Moreover, the resulting substrate necessarily has an upper layer having a first silicon crystal, and a lower layer having a second silicon crystal. Therefore, unlike the SIMOX substrate which may include only one single silicon crystal layer (although, heavily damaged), the substrate formed by the cladding process includes two silicon crystals which may have a different crystal orientation from one another.

In addition, unlike the substrates formed by the cladding process, the claimed substrate does not require the bonding together of two separate silicon crystals. Instead, the claimed device may be formed of a single silicon crystal, and may, therefore, have a same crystal orientation. Thus, the claimed device has a higher substrate quality than conventional devices (Application at page 5, lines 2-10).

Clearly, Ohata does not teach or suggest these novel features. Indeed, Ohata is merely directed to a wafer bonding process which, as explained above, is completely different than the claimed invention. Further, Ohata does not even address at least one of the problems (e.g., defects in the silicon of the SOI region caused by the SIMOX process) which the claimed substrate is intended to address.

Specifically, Ohata merely discloses a device formed according to a process which is

similar to the cladding process described above. Specifically, the Ohata device includes a first monocrystalline silicon plate, an insulating layer embedded in the first silicon plate, and a second monocrystalline silicon plate bonded to the first silicon plate (Ohata at Abstract; Figure 8A; col. 4, lines 1-47).

Therefore, as discussed above with respect to the cladding process, the Ohata device will necessarily include two silicon crystals (e.g., upper and lower wafers). That is the upper and lower wafers which are bonded together are not formed of the same silicon crystal. This is completely different from the claimed substrate (or device) in which an upper portion and lower portion of single silicon crystal are formed of the same silicon crystal. Therefore, the Ohata device is clearly inferior to the claimed invention.

Further, Applicant respectfully submits that the unique features of the claimed substrate (e.g., an upper portion including crystallized epitaxial silicon) clearly result in a "distinct structure being produced". Specifically, Applicant respectfully submits that the claimed substrate results in the upper portion and the lower portion of the single crystal silicon being formed of the same silicon crystal. This novel feature is clearly not taught or suggested by Ohata.

Therefore, Applicant submits that Ohata does not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

B. The Tanaka Reference

The Examiner alleges that Tanaka would have been combined with Ohata to form the claimed invention (as recited in claims 37-39 and 43-44). Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Tanaka discloses a method of forming a hybrid element on a SIMOX wafer. Specifically, a silicon substrate 3 is exposed by selectively removing a silicon layer 1 and an insulating layer 2 from a silicon-on-insulator (SOI) substrate. The desired semiconductor elements 11 are respectively formed on the exposed silicon substrate 3 and the silicon layer 1 (Tanaka at Abstract).

However, Applicant submits that these references would not have been combined as

alleged by the Examiner. Indeed, these references are directed to different matters and different problems. Specifically, Ohata is merely directed to a cladding type process of forming an insulating layer in a substrate, whereas Tanaka is directed to a well-known SIMOX process for forming a logic circuit and memory cell on a substrate. Clearly, these references teach away from each other and would not have been combined by one of ordinary skill in the art.

Further, Applicant submits that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, the Examiner supports the combination by merely stating that "[i]t would have been obvious ... to form a DRAM memory device on the silicon bulk and a MOSFET logic device on the SOI region, as taught by Tanaka, in Ohata et al.'s device in order to provide a hybrid device wherein the DRAM can operate at high speed with less power consumption and the logic circuits are adequately isolated" which is merely a conclusory statement and insufficient to support the combination of these disparate references.

Moreover, like Ohata, Tanaka does not teach or suggest "*wherein said upper portion of said single crystal silicon comprises crystallized epitaxial silicon which is grown from said lower portion of said single crystal silicon such that said upper portion and said lower portion comprise a same silicon crystal*", as recited, for example, in claims 29, 41 and 45- 46.

As noted above, unlike conventional substrates, the claimed invention includes an upper portion of single crystal silicon which includes crystallized epitaxial silicon grown from the lower portion, such that an upper portion and lower portion of single silicon crystal which are formed of the same silicon crystal (Application at page 9, lines 4-22). Therefore, the claimed invention provides superior characteristics over conventional substrates which are formed by either the SIMOX (e.g., see Application at page 5, lines 2-10) or cladding process.

Clearly, Tanaka does not teach or suggest these novel features. Indeed, Tanaka is merely directed to a SIMOX process which, as explained above, is completely different than the claimed invention. Further, SIMOX does not even address at least one of the problems (e.g., defects in the silicon of the SOI region caused by the SIMOX process) which the claimed substrate is intended to address.

Specifically, as noted above, it is well known that the high energy implantation of the SIMOX process results in a very high defect count per unit area (i.e., defect density) in the

silicon over the insulation layer (Application at page 5, lines 2-6). Moreover, these defects are spread out all over the portion of the silicon over the insulation layer. In other words, the defects are not localized and cannot be removed. Therefore, such conventional devices do not include an upper portion of single crystal silicon which is substantially devoid of a defective region.

The claimed invention, on the other hand, has an upper portion of single crystal silicon which includes crystallized epitaxial silicon grown from the lower portion. As a result, the defective regions are localized (e.g., near the end portions of the insulator layer and near the seam where the epitaxially grown silicon comes together over the insulator layer). Therefore, the defective regions may be easily removed. As a result, the claimed invention includes an upper portion of single crystal silicon which is substantially devoid of a defective region.

This is feature is clearly not attainable using the SIMOX process of Tanaka. Therefore, Tanaka certainly does not teach or suggest this novel feature of the claimed invention.

Therefore, Applicant submits that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 29-39 and 41-57, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0510.

Respectfully Submitted,

Date: 8/20/03

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CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that the foregoing Amendment was filed by facsimile with the United States Patent and Trademark Office, Examiner Ori Nadav, Group Art Unit # 2811 at fax number 703-872-9318 this 20th day of August, 2003.

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